

Low Power High Speed Carry Select Adder Using GDI-MUX

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Abstract – This paper discusses about the performance characteristics of a Full Adder based Carry Select Adder using various logics and also GDI-MUX technique. The adders are used in many data path applications and also the area, power consumption and delay in the design can be reduced. The proposed technique is the GDI-Mux which enables the reduction of above mentioned parameters and also reduce the number of transistors. The Full Adder based Carry Select Adder designed in Complementary Pass Transistor Logic, Complementary Metal Oxide Semiconductor Logic and Gate Diffusion Input – Mux and they are compared and the most efficient technique is identified.

Index Terms – GDI Technique, Design of carry select adder for low power and high speed VLSI applications.

1. INTRODUCTION

The history of transistor dates back to the mid1920s when devices to control current in solid-state diodes and convert them into triodes were attempted to be invented .Very-Large-Scale-Integration(VLSI) is the process of creating an Integrated Circuit by combining thousands of transistors into a single chip. Before the introduction of VLSI IC's had only a limited set of functions they could perform. A well established domain in VLSI is low power design. It has undergone many changes through transistor sizing, clock gating, voltage scaling and so on. For many designs, power dissipation is as important as timing. Requirements for lower power consumption continue to increase significantly as components become battery-powered, smaller and require more functionality. Now a day's power is the primary concerned due to the remarkable growth and success in the field of personal computing devices and wireless communication system which demand high speed computation and complex functionality with low power

consumption. The motivations for reducing power consumption differ application to application. The need for lower power systems is being driven by many market segments. The software used is DSCH and MICROWIND.

2. CARRY SELECT ADDER

Carry Select Adder is one of the fast adders. It reduces the propagation and can perform fast additions. A 4-bit Carry Seley Adder is desinged using two Ripple Carry Adders and Multiplexers. The first 4-bit Ripple Carry Adder has “Zero” carry-in and the second 4-bit Ripple Carry Adder has “One” carry-in.

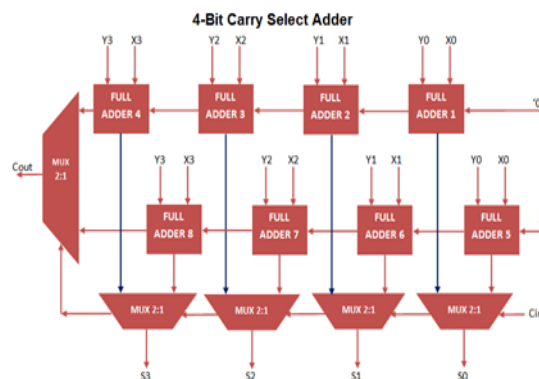


Fig. 1 Carry Select Adder

Four Multiplexers are used to determine the sum output of the Carry Select Adder and One Multiplexer to determine the Carry-out output . The Selection line to the Multiplexer is Cin. The block diagram of a Carry Select Adder is

3. PROPOSED TECHNIQUE

The Gate Diffusion Input (GDI) technique offers realization of extensive variety of logic functions using simple two transistor based circuit arrangement. This scheme is appropriate for fast and low power circuit design, which reduces number of MOS transistors as compared to CMOS and other existing low power techniques, while the logic level swing and static power dissipation improves.

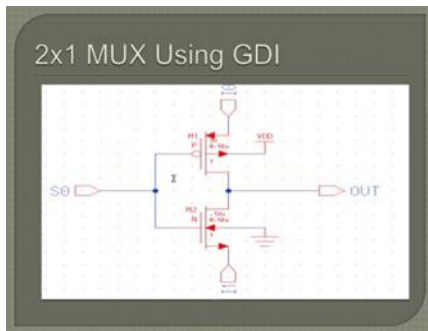


Fig. 2. 2*1 MUX using GDI

The Carry Select Adder is designed using a Full Adder in CMOS, CPL and GDI-MUX techniques. 28,20,12 transistors are required to design a Full Adder in CMOS, CPL and GDI-MUX technique. The proposed technique is the GDI-MUX technique. The circuit of a Full Adder in GDI-MUX is

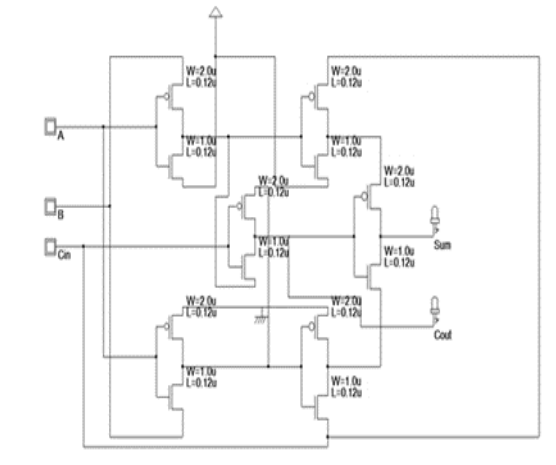


Fig. 3 GDI-MUX-Full Adder

A Full Adder has three inputs and two outputs. The inputs are A, B and Cin and the outputs are Sum and Cout. In GDI-MUX Full adder the Cout is obtained as A ANDING B if Cin is "0" and Cout is obtained as A ORING B if Cin is "1". Also the Sum is obtained as A ORING B ORING CIN if the Cout is "0" and Sum is obtained as A ANDING B ANDING Cin if Cout is "1". The above circuit is desinged in DSCH and made into a module which is further used in the design of the Carry Select Adder. The Carry Select Adder in GDI-MUX is

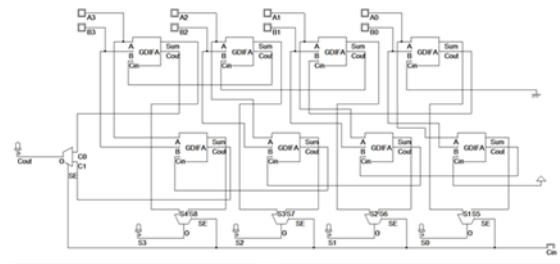


Fig. 3 GDI-MUX-Carry Select Adder

4. SIMULATION RESULTS

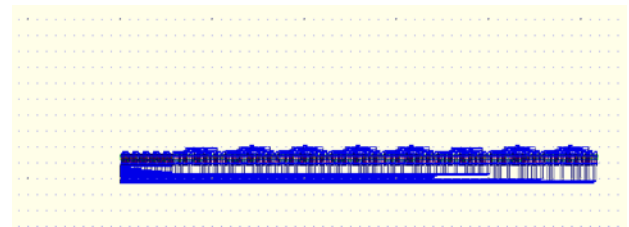


Fig. 4 Layout of CMOS carry select adder

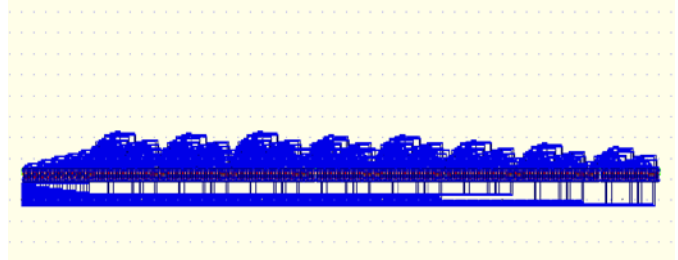


Fig.5 Layout of CPL-Carry Select Adder

5. ANALYSIS

The design of Carry Select Adder in CMOS, CPL and GDI-MUX technique is simulated in MICROWIND software to obtain the delay and power consumptions of the respective circuits. Also the number of transistors, Area are compared and tabulated as follows

Logics	Technology	#. Tr	Power	Area	Delay
CMOS -CSA	90nm	264	16.815μW	3059.7 μm ²	1.16 Ns
CPL- CSA	90nm	180	43.573μW	4729.5 μm ²	0.916 ns

GDI-MUX-CSA	90nm	106	9.24μW	2161.5μm ²	0.493 ns
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TABLE.1 PARAMETRIC ANALYSIS

6. CONCLUSION

From the comparison table, it seen that the GDI-MUX technique uses less number of Transistors which in turn reduces the power consumption due to reduced area . The complexity of the circuit is also reduced . Thus the proposed technique is an effective technique.

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